RESUME



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❖ Qualification : PhD

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* Educational qualification

<u>Degree</u>	<u>University</u>	Year of completion	Class /Grade
PhD	Pacific Academy of Higher Education and Research University, Udaipur	2019	
Diploma In Management	Indira Gandhi Open University	June 2005	
M.E(Electronics)	Shivaji University Kolhapur	January 1995	First class 67%
B.E (Electronics & Communication)	Karnataka Univeristy Dharwar	August 1988	First class distinction 70%
P.U.C	Karnataka Pre University board	June 1984	First class 84%
S.S.L.C	Karnataka Secondary Board of Education	May 1982	First class 74%

❖ Professional Qualification: 10 Years Industry and 14 years teaching

Organisation/Institution	Designation	Period	
		From	To
BLDEA's College of Engg and Technology Bijapur	Lecturer in Electronics & Communication Dept	19.08.1988	20.08.1989
D.Y Patil College of Engg & Technology Kolhapur	Lecturer in Computer Science Dept	21.08.1989	20.08.1991
BLDEA's College of Engg and Technology Bijapur	Lecturer in Computer Science Dept	02.09.1991	14.09.1993
PDA College of Engg Gulbarga	Lecturer in Electronics Dept	10.10.1995 year.	for 1 academic
BK Birla's Vasavadatta Cement Sedam	Sr Engr(EDP)	25.9.1996	17.08.2006
Karshak Engg College Hyderabad	Asst Professor in Electronics Dept	22.08.2006	25.04.2008
RGM Group SyamalaDevi Institute of Technology for Women Nandyal A.P	Assoc Professor and Head of Electronics Dept	07.06.2008	15.10 2009
Bhagwan Mahavir ollege of Engg and Technology Surat Gujarat	Head of the Electronics Department	22.07.2010	10.08.2015
Biluru Gurubasava Mahaswamiji Institute of Technology Mudhol,Karnataka	Professor ,Department of Electronics and Communication	25.10.2021	till date

- * Additional Qualification: Diploma in Management from IGNOU
- * Papers published in conferences or Journals:

1.Design and Implementation of FPGA based Linear All Digital Phase Locked Loop

Published in: International conference on Green Computing communication and Electrical Engineering (ICGCCEE), 2014

Date of Conference: 6-8 March 2014 Page no 630 - 633

INSPEC Accession Number:14665797 DOI:

10.1109/ICGCCEE.2014.6922342 Publisher:IEEE

2. FIR for All digital Phase Locked Loops

Published in International Journal of Multidisciplinary Educational Research IJMER; ISSN: 2277-7881; IF-2.735; IC V:5.16; Vol 3, Issue 3(6), April 2014

3.DESIGN AND MODELLING HILBERT TRANSFORM BASED PHASE DETECTOR FOR ALL DIGITAL PHASE LOCKED LOOP

Published in INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY ISSN: 2277-9655 DOI: 10.5281/zenodo.51007, page no 134 - 138

4.IIR FILTER IN ALL DIGITAL PHASE LOCKED LOOP

Published in the Proceeding Of 4th International Conference on Futuristic Trends in Engineering and Technologies (ICFTET-2016) Date: 30th June, 2016 Goa; page no 83-88

5.A Numerically controlled oscillator for all Digital Phase Locked Loop Published in International Journal of Engineering Trends and Technology (IJETT), V38(4),186-189 August 2016. ISSN:2231-5381. www.ijettjournal.org. published by seventh sense research group

- ❖ <u>Additional Skills</u>: I have worked as Placement officer and have organized conferences and workshops in my tenure.
- ❖ Filed a Patent: Application No:202041046305 IOT BASED OPTIMIZATION OF SOLAR POWER GENERATION FOR EFFICIENT MANAGEMENT OF SMART CITIES
- Computer Hardware and software skills:
 - <u>Hardware</u>: Personal computers and printers troubleshooting and maintenance.
 - o Certificate course in Computer maintenance and troubleshooting.
 - Software: Database: Oracle 7x Foxpro

Operating system: Presently working on UNIX and windows
Programming: C,Pro*c,PLSQL,SQL SQl Reports

C++,malab xilinx

Applications worked on: Payroll system ;

Stores Inventory system;

Purchase system; Accounting system:

Computer Maintenance Management;

Mines tyre management; Co operative stores finance;